CLAIMS

What is claimed is:

1. A clock and data recovery device for generating data samples in response to data having jitter, said device including:

sampling circuitry coupled and configured to receive the data and to employ 2x oversampling using a data sampling clock and an edge sampling clock to generate the data samples;

clock generation circuitry configured to generate the data sampling clock in response to at least one control signal and to assert the data sampling clock to the sampling circuitry, wherein the phase of said data sampling clock is determined by the control signal;

phase detection circuitry configured to generate feedback indicative of the amount of the jitter and of phase error between the data sampling clock and the data; and

clock control circuitry, coupled and configured to generate the control signal in response to the feedback and to assert the control signal to the clock generation circuitry, wherein the control signal is at least substantially independent of the amount of the jitter over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of the phase error between the data sampling clock and the data over the time interval.

2. The device of claim 1, wherein the clock generation circuitry is a voltage controlled oscillator, the clock control circuitry includes a charge pump circuit, and the charge pump circuit is configured to generate a charge pump current in response to the feedback and to generate the control signal in response to the charge pump current, wherein the charge pump current has an average current value, I_{avg}, that is at least substantially independent of the amount of the jitter over said each time interval over which ϕ_{av} is nonzero, where I_{avg} is an average of instantaneous values of the charge pump current over the time interval.

3. The device of claim 2, wherein the charge pump circuit is configured to generate the charge pump current such that said charge pump current has an absolute value that is proportional to the amount of the jitter.

4. The device of claim 2, wherein the average current value, I_{avg}, is independent of the amount of the jitter over said each time interval over which ϕ_{av} is nonzero.

5. The device of claim 2, wherein the feedback is indicative of a sequence of control bit pairs, a first bit in each of the pairs is indicative of whether the phase error between the data sampling clock and the data is positive, a second bit in each of the pairs is indicative of whether said phase error is negative, and the charge pump circuit includes:

a first node coupled to receive a first signal indicative of the first bit of each of the control bit pairs;

a second node coupled to receive a second signal indicative of the second bit of each of the control bit pairs;

delay circuitry coupled to receive the first signal and the second signal and configured to assert in response thereto a first delayed signal indicative of the first bit of each of the control bit pairs and a second delayed signal indicative of the second bit of each of the control bit pairs;

a third node; and

additional circuitry, coupled to the first node, the second node, the delay circuitry, and the third node, and configured to source a positive current to the third node when one of the control bit pairs indicates positive phase error but does not indicate negative phase error between the data sampling clock and the data, and to sink a current from the third node when one of the control bit pairs indicates negative phase error but does not indicate positive phase error between the data sampling clock and the data.

6. The device of claim 5, wherein the second signal is indicative of the complement of the second bit of each of the charge pump control bit pairs, the delay circuitry includes a first inverter whose input is the first node and a second inverter whose input is the second node, the first inverter has an output coupled to assert the first delayed signal to the additional circuitry, and the second inverter has an output coupled to assert the second delayed signal to the additional circuitry.

7. The device of claim 1, wherein the clock generation circuitry is configured to generate a second clock whose phase is fixed relative to the data sampling clock in response to said at least one control signal and to generate the edge sampling clock by applying variable delay to the second clock such that the edge sampling clock has a varying phase that defines a dead zone having a dead zone width, and wherein the feedback includes a jitter signal indicative of the amount of the jitter, the clock control circuitry includes a dead zone width control circuit configured to generate the jitter signal, and the clock generation circuitry is configured to adjust the dead zone width in response to the jitter signal.

8. The device of claim 7, wherein the data defines a data eye and the clock generation circuitry is configured to adjust the dead zone width in response to the jitter signal to cause edges of the dead zone to track boundaries of the data eye.

9. The device of claim 7, wherein the clock generation circuitry is configured to generate a third clock and to generate the data sampling clock by applying variable delay to the third clock, and

the dead zone width control circuit is configured to generate a sequence of counts and to generate the jitter signal in response to the sequence of counts, wherein each of the counts is indicative of the number of times that the clock generation circuitry changes the phase of the third clock during a predetermined number of valid transitions of the data.

10. The device of claim 9, wherein the clock generation circuitry is configured to increase the dead zone width in response to values of the jitter signal indicative of an increasing sequence of the counts, and to decrease the dead zone width in response to values of the jitter signal indicative of a decreasing sequence of the counts.

11. The device of claim 1, wherein the data sampling clock has frequency equal to f/N, where f is the bit rate of the data, and N is an integer greater than one.

12. A clock and data recovery device for generating data samples in response to data having jitter, said device including:

sampling circuitry coupled and configured to receive the data and to employ 2x oversampling using a data sampling clock and an edge sampling clock to generate the data samples;

clock generation circuitry configured to generate the data sampling clock in response to a charge pump current and to assert the data sampling clock to the sampling circuitry, wherein the phase of said data sampling clock is determined by the charge pump current; and

clock control circuitry, coupled and configured to generate feedback indicative of the amount of the jitter and of phase error between the data sampling clock and the data, to generate the charge pump current in response to the feedback, and to assert at least one of the charge pump current, and a control signal determined by the charge pump current, to the clock generation circuitry, wherein the charge pump current has an average current value, I_{avg}, that is at least substantially independent of the amount of the jitter over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of the phase error between the data sampling clock and the data over the time interval, and I_{avg} is an average of instantaneous values of the charge pump current over said time interval.

13. The device of claim 12, wherein the average current value, I_{avg}, is independent of the amount of the jitter over said each time interval over which ϕ_{av} is nonzero.

14. The device of claim 12, wherein the clock control circuitry is configured to generate the charge pump current such that said charge pump current has an absolute value that is proportional to the amount of the jitter.

15. The device of claim 12, wherein the clock generation circuitry is configured to generate a second clock whose phase is fixed relative to the data sampling clock in response to the charge pump current and to generate the edge sampling clock by applying variable delay to the second clock such that the edge sampling clock has a varying phase that defines a dead zone having a dead zone width, and wherein the feedback includes a jitter signal indicative of the amount of the jitter, the clock control circuitry includes a dead zone width control circuit configured to generate the jitter

signal, and the clock generation circuitry is configured to adjust the dead zone width in response to the jitter signal.

16. The device of claim 15, wherein the data defines a data eye and the clock generation circuitry is configured to adjust the dead zone width in response to the jitter signal to cause edges of the dead zone to track boundaries of the data eye.

17. The device of claim 15, wherein the clock control circuitry is configured to generate the charge pump current in response to the jitter signal such that said charge pump current has an absolute value that is proportional to the amount of the jitter.

18. The device of claim 15, wherein the clock control circuitry is configured to generate the charge pump current in response to the jitter signal such that the average current value, I_{avg}, is at least substantially independent of the amount of the jitter and the dead zone width.

19. The device of claim 15, wherein the clock generation circuitry is configured to generate a third clock and to generate the data sampling clock by applying variable delay to the third clock, and

the dead zone width control circuit is configured to generate a sequence of counts and to generate the jitter signal in response to the sequence of counts, wherein each of the counts is indicative of the number of times that the clock generation circuitry changes the phase of the third clock during a predetermined number of valid transitions of the data.

20. The device of claim 19, wherein the clock generation circuitry is configured to increase the dead zone width in response to values of the jitter signal indicative of an increasing sequence of the counts, and to decrease the dead zone width in response to values of the jitter signal indicative of a decreasing sequence of the counts.

21. The device of claim 12, wherein the clock control circuitry includes a charge pump circuit configured to generate the charge pump current, the device also includes a frequency acquisition loop coupled to receive a reference clock having a reference frequency, and the device is operable in a frequency locking mode in which

the charge pump circuit is decoupled from the clock generation circuitry and the frequency acquisition loop is coupled to the clock generation circuitry,

the frequency acquisition loop generates a clock control signal in response to the reference clock and the data sampling clock, and

the frequency acquisition loop asserts the clock control signal to the clock generation circuitry to cause the frequency of the data sampling clock to match the reference frequency.

22. The device of claim 12, wherein the clock generation circuitry is a voltage controlled oscillator, and the clock control circuitry is configured to assert a control voltage, determined by the charge pump current, to the clock generation circuitry.

23. The device of claim 12, wherein the feedback is indicative of a sequence of control bit pairs, a first bit in each of the pairs is indicative of whether the phase error between the data sampling clock and the data is positive, a second bit in each of the pairs is indicative of whether said phase error is negative, the clock control circuitry includes a charge pump circuit configured to generate the charge pump current, and the charge pump circuit includes:

a first node coupled to receive a first signal indicative of the first bit of each of the control bit pairs;

a second node coupled to receive a second signal indicative of the second bit of each of the control bit pairs;

delay circuitry coupled to receive the first signal and the second signal and configured to assert in response thereto a first delayed signal indicative of the first bit of each of the control bit pairs and a second delayed signal indicative of the second bit of each of the control bit pairs;

a third node; and

additional circuitry, coupled to the first node, the second node, the delay circuitry, and the third node, and configured to source a positive current to the third node when one of the control bit pairs indicates positive phase error but does not indicate negative phase error between the data sampling clock and the data, and to sink a current from the third node when one of the control bit pairs indicates negative phase error but does not indicate positive phase error between the data sampling clock and the data.

24. The device of claim 23, wherein the second signal is indicative of the complement of the second bit of each of the charge pump control bit pairs, the delay circuitry includes a first inverter whose input is the first node and a second inverter whose input is the second node, the first inverter has an output coupled to assert the first delayed signal to the additional circuitry, and the second inverter has an output coupled to assert the second delayed signal to the additional circuitry.

25. The device of claim 12, wherein the data sampling clock has frequency equal to f/N, where f is the bit rate of the data, and N is an integer greater than one.

26. A clock and data recovery device for generating data samples in response to data having jitter and defining a data eye, wherein the data has a bit period, said device including:

a data loop; and

a dead zone width control loop,

wherein the data loop includes sampling circuitry and clock generation circuitry, the sampling circuitry is coupled and configured to receive the data and employ 2x oversampling using a data sampling clock and an edge sampling clock to generate the data samples, and the clock generation circuitry is configured to generate a first clock having a first variable phase and second clock having second variable phase, to maintain the difference between the first variable phase and the second variable phase at a value at least substantially equal to 180 degrees, where 180 degrees corresponds to one half of the bit period, to generate the data sampling clock by delaying the first clock by a first variable delay, to maintain the phase of the data sampling clock at the center of the data eye, and to generate the edge sampling clock by applying a sequence of second and third variable delays to the second clock, where the difference between each of the second variable delays and the first variable delay contemporaneous therewith is a fixed positive value, and the difference between each of the third variable delays and the first variable delay contemporaneous therewith is a fixed negative value, so that the edge sampling clock has a varying phase that defines a dead zone having a dead zone width,

wherein the clock generation circuitry is configured to generate the first clock in response to a control signal such that phase of said data sampling clock is determined

by the control signal, and the data loop is configured to operate in response to the edge sampling clock and the data samples to generate feedback indicative of the amount of the jitter and of phase error between the data sampling clock and the data, and to generate the control signal in response to the feedback such that the control signal is at least substantially independent of the amount of the jitter over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of the phase error between the data sampling clock and the data over the time interval, and

wherein the dead zone width control loop is configured to generate a jitter signal in response to the feedback and to control generation of the edge sampling clock in response to the jitter signal to cause edges of the dead zone to track boundaries of the data eye, wherein the jitter signal is indicative of the amount of the jitter.

27. The device of claim 26, wherein the clock generation circuitry is a voltage controlled oscillator, the clock control circuitry includes a charge pump circuit, and the charge pump circuit is configured to generate a charge pump current in response to the feedback and to generate the control signal in response to the charge pump current, and wherein the dead zone width control loop is configured to control generation of the charge pump current in response to the jitter signal such that said charge pump current has an absolute value that is proportional to the amount of the jitter.

28. The device of claim 27, wherein the charge pump current has an average current value, I_{avg}, that is an average of instantaneous values of the charge pump current over said each time interval over which ϕ_{av} is nonzero, and wherein the dead zone width control loop is configured to control generation of the charge pump current in response to the jitter signal such that the average current value, I_{avg}, is at least substantially independent of the amount of the jitter and the dead zone width over said each time interval over which ϕ_{av} is nonzero.

29. The device of claim 26, wherein the feedback is indicative of a sequence of control bit pairs, a first bit in each of the pairs is indicative of whether the phase error between the data sampling clock and the data is positive, a second bit in each of the pairs is indicative of whether said phase error is negative, and the charge pump circuit includes:

a first node coupled to receive a first signal indicative of the first bit of each of the control bit pairs;

a second node coupled to receive a second signal indicative of the second bit of each of the control bit pairs;

delay circuitry coupled to receive the first signal and the second signal and configured to assert in response thereto a first delayed signal indicative of the first bit of each of the control bit pairs and a second delayed signal indicative of the second bit of each of the control bit pairs;

a third node; and

additional circuitry, coupled to the first node, the second node, the delay circuitry, and the third node, and configured to source a positive current to the third node when one of the control bit pairs indicates positive phase error but does not indicate negative phase error between the data sampling clock and the data, and to sink a current from the third node when one of the control bit pairs indicates negative phase error but does not indicate positive phase error between the data sampling clock and the data.

30. The device of claim 29, wherein the second signal is indicative of the complement of the second bit of each of the charge pump control bit pairs, the delay circuitry includes a first inverter whose input is the first node and a second inverter whose input is the second node, the first inverter has an output coupled to assert the first delayed signal to the additional circuitry, and the second inverter has an output coupled to assert the second delayed signal to the additional circuitry.

31. The device of claim 26, the dead zone width control circuit is configured to generate a sequence of counts and to generate the jitter signal in response to the sequence of counts, wherein each of the counts is indicative of the number of times that the clock generation circuitry changes the phase of the second signal during a predetermined number of valid transitions of the data.

32. The device of claim 31, wherein the clock generation circuitry is configured to increase the dead zone width in response to values of the jitter signal indicative of an increasing sequence of the counts, and to decrease the dead zone width in response to values of the jitter signal indicative of a decreasing sequence of the counts.

33. The device of claim 26, wherein the data sampling clock has frequency equal to f/N, where f is the bit rate of the data, and N is an integer greater than one.

34. A jitter estimating circuit for use in an clock and data recovery device configured to generate samples of data having jitter using a data sampling clock, where the clock and data recovery device is configured to generate the data sampling clock by applying variable delay to a first clock in response to feedback indicative of phase error between the data sampling clock and the data, said circuit including:

counter circuitry configured to generate a sequence of counts in response to the feedback, wherein each of the counts is indicative of the number of times that the clock and data recovery device changes the phase of the first clock during a predetermined number of valid transitions of the data; and

decision logic, coupled to the counter circuitry and configured to generate code words in response to the counts, wherein the counts have values in a range of count values, the range is partitioned into segments, and each of the code words is generated in response to one of the counts and indicates one of the segments to which said one of the counts belongs.

35. The circuit of claim 34, wherein the range of count values is partitioned into five segments.

36. The circuit of claim 34, wherein the clock and data recovery device is configured to generate a second clock whose phase is fixed relative to the data sampling clock and to generate an edge sampling clock by applying variable delay to the second clock such that the edge sampling clock has a varying phase that defines a dead zone having a dead zone width, and also including:

additional circuitry coupled to the decision logic and configured to generate at least one dead zone width control signal in response to the code words.

37. The circuit of claim 36, wherein the range of count values is partitioned into at least three segments, and

the additional circuitry has a state in which it generates the dead zone width control signal to have a value indicating that the dead zone width should decrease in

response to each of the code words indicating one of counts in a first one of the segments, generates the dead zone width control signal to have a value indicating that the dead zone width should not change in response to each of the code words indicating one of counts in a second one of the segments, and generates the dead zone width control signal to have a value indicating that the dead zone width should increase in response to each of the code words indicating one of counts in a third one of the segments.

38. A transceiver, including:

transmitter circuitry; and

receiver circuitry coupled and configured to receive data having jitter, and including a clock and data recovery device for generating data samples in response to the data, said clock and data recovery device including:

sampling circuitry coupled and configured to receive the data and to employ 2x oversampling using a data sampling clock and an edge sampling clock to generate the data samples;

clock generation circuitry configured to generate the data sampling clock in response to at least one control signal and to assert the data sampling clock to the sampling circuitry, wherein the phase of said data sampling clock is determined by the control signal;

phase detection circuitry configured to generate feedback indicative of the amount of the jitter and of phase error between the data sampling clock and the data; and

clock control circuitry, coupled and configured to generate the control signal in response to the feedback and to assert the control signal to the clock generation circuitry, wherein the control signal is at least substantially independent of the amount of the jitter over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of the phase error between the data sampling clock and the data over the time interval.

39. A transceiver, including:

transmitter circuitry; and

receiver circuitry coupled and configured to receive data having jitter, and including a clock and data recovery device for generating data samples in response to the data, said clock and data recovery device including:

sampling circuitry coupled and configured to receive the data and to employ 2x oversampling using a data sampling clock and an edge sampling clock to generate the data samples;

clock generation circuitry configured to generate the data sampling clock in response to a charge pump current and to assert the data sampling clock to the sampling circuitry, wherein the phase of said data sampling clock is determined by the charge pump current; and

clock control circuitry, coupled and configured to generate feedback indicative of the amount of the jitter and of phase error between the data sampling clock and the data, to generate the charge pump current in response to the feedback, and to assert at least one of the charge pump current, and a control signal determined by the charge pump current, to the clock generation circuitry, wherein the charge pump current has an average current value, I_{avg}, that is at least substantially independent of the amount of the jitter over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of the phase error between the data sampling clock and the data over the time interval, and I_{avg} is an average of instantaneous values of the charge pump current over said time interval.

40. A transceiver, including:

transmitter circuitry; and

receiver circuitry coupled and configured to receive data having jitter and defining a data eye, and including a clock and data recovery device for generating data samples in response to the data, said clock and data recovery device including a data loop and a dead zone width control loop, wherein the data has a bit period, and

wherein the data loop includes sampling circuitry and clock generation circuitry, the sampling circuitry is coupled and configured to receive the data and employ 2x oversampling using a data sampling clock and an edge sampling clock to generate the data samples, and the clock generation circuitry is configured to generate a first clock having a first variable phase and second clock having second variable phase, to maintain the difference between the first variable phase and the second variable phase at a value at least substantially equal to 180 degrees, where 180 degrees

corresponds to one half of the bit period, to generate the data sampling clock by delaying the first clock by a first variable delay, to maintain the phase of the data sampling clock at the center of the data eye, and to generate the edge sampling clock by applying a sequence of second and third variable delays to the second clock, where the difference between each of the second variable delays and the first variable delay contemporaneous therewith is a fixed positive value, and the difference between each of the third variable delays and the first variable delay contemporaneous therewith is a fixed negative value, so that the edge sampling clock has a varying phase that defines a dead zone having a dead zone width,

wherein the clock generation circuitry is configured to generate the first clock in response to a control signal such that phase of said data sampling clock is determined by the control signal, and the data loop is configured to operate in response to the edge sampling clock and the data samples generated by the sampling circuitry to generate feedback indicative of the amount of the jitter and of phase error between the data sampling clock and the data, and to generate the control signal in response to the feedback such that the control signal is at least substantially independent of the amount of the jitter over each time interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of the phase error between the data sampling clock and the data over the time interval, and

wherein the dead zone width control loop is configured to generate a jitter signal in response to the feedback and to control generation of the edge sampling clock in response to the jitter signal to cause edges of the dead zone to track boundaries of the data eye, wherein the jitter signal is indicative of the amount of the jitter.

41. A method for sampling data having jitter, including the steps of:

(a) generating at least one sampling clock in response to a charge pump current, where at least one said sampling clock is a data sampling clock and the charge pump current determines the phase of the data sampling clock;

(b) generating data samples by sampling the data using the data sampling clock; and

(c) generating the charge pump current in response to feedback, where the feedback is indicative of phase error between the data sampling clock and the data, the feedback is also indicative of the jitter, the charge pump current has an average current value that is at least substantially independent of the amount of the jitter over each time

interval over which ϕ_{av} is nonzero, where ϕ_{av} is an average of instantaneous values of said phase error over the time interval, and the average current value is an average of instantaneous values of the charge pump current over said time interval.

42. The method of claim 41, wherein the charge pump current is a positive current, I_P, when the phase error is negative, the charge pump current is a negative current, $-(I_P)$, when the phase error is positive, and step (c) includes the step of controlling the absolute value of the charge pump current to cause said absolute value be proportional to the jitter.

43. The method of claim 41, wherein another one of said at least one sampling clock generated during step (a) is a first clock whose phase is determined by the charge pump current, and wherein step (c) includes the steps of:

modulating the first clock to generate an edge sampling clock such that said edge sampling clock defines a dead zone having a dead zone width;

generating additional samples of the data in response to the edge sampling clock; and

generating the feedback in response to the data samples and the additional data samples.

44. The method of claim 41, wherein the data determines a data eye, and step (c) includes the step of automatically adjusting the dead zone width to cause edges of the dead zone to track boundaries of the data eye.